



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/342,235	06/29/1999	YASUHIKO TAKEMURA	0756-1980ELE	6257
31780	7590	06/02/2005	EXAMINER	
ERIC ROBINSON PMB 955 21010 SOUTHBANK ST. POTOMAC FALLS, VA 20165			SEFER, AHMED N	
			ART UNIT	PAPER NUMBER
			2826	

DATE MAILED: 06/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.		Applicant(s)	
	09/342,235		TAKEMURA, YASUHIKO	
	Examiner		Art Unit	
	A. Sefer		2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 March 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 6-11 and 13-25 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 6-11 is/are allowed.
- 6) ☒ Claim(s) 13-25 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>3/14/2005</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

1. The amendment filed on March 14, 2005 has been entered; no new claims have been introduced.

Priority

2. Submission of the certified translation of the Japanese Priority Document (JP 3-296331) is acknowledged. Therefore, Yamazaki et al. USPN 6,331,723 is not available as a prior art.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 13-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. ("Yamazaki") USPN 5,905,555 in view of Takahata ("Takahata") JP 63-76474.

Yamazaki discloses (see fig. 8 and col. 10, lines 36-40) a semiconductor device comprising a substrate 11 having an insulating surface; at least first and second semiconductor islands comprising polysilicon (as in claims 14, 17 and 21) formed over said substrate wherein each of the semiconductor islands has a channel region 28, 28' and a pair of impurity regions 34, 34'; a first and a second gate insulating film formed over said semiconductor island, respectively; at least first and second gate electrodes 40, 40' formed over said first and second semiconductor islands respectively with said first and second gate insulating films interposed therebetween; an interlayer insulating film 37 formed over a wiring (as in claims 16 and 19); a

Art Unit: 2826

smoothing film 39 formed over a wiring (as in claims 20 and 23); a pixel electrode formed over said interlayer insulating film (as in claim 16) or a pixel electrode formed over said smoothing film (as in claim 20) and electrically connected to one of the pair of the impurity regions of the second semiconductor island; wherein the first semiconductor island is a part of an NTFT and the second semiconductor island is a part of a PTFT, but lacks anticipation of a wiring connecting one of the first impurity regions of the first semiconductor island with the second gate electrode.

Takahata discloses in figs. 2 and 6 a semiconductor device comprising a substrate 1 having an insulating surface; at least first and second semiconductor islands 2 comprising polysilicon (as in claims 14 and 17) formed directly on said insulating surface wherein each of the semiconductor islands has a channel region and a pair of impurity regions 5; a first and a second gate insulating film 3 formed over said semiconductor island, respectively; at least first and second gate electrodes 4 formed over said first and second semiconductor islands respectively with said first and second gate insulating films interposed therebetween; a wiring for electrically connecting one of the impurity regions of the first semiconductor island with the second gate electrode (fig. 2); an interlayer insulating film 3 formed over a wiring (as in claims 16 and 19); and wherein the first semiconductor island is a part of an NTFT and the second semiconductor island is a part of PTFT (abstract).

Therefore, in view of Takahata's teachings, one having an ordinary skill in the art at the time the invention was made would be motivated to modify Yamazaki's device by incorporating Takahata teachings since that would enhance speed as taught by Takahata.

Art Unit: 2826

As to claims 15, 18 and 22, Yamazaki discloses a data line electrically connected to one impurity region of an NTFT.

As for claims 24 and 25, Takahata discloses in fig. 6 a voltage supply line 8 electrically connected to the other one of the pair of the impurity regions of the second semiconductor island.

Allowable Subject Matter

5. Claims 6-11 are allowed.

TECHNOLOGY CENTER 2800
NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (571) 272-1921.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANS
May 22, 2005